REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on August 15, 2003.

Prior to this Amendment, claims 24, 26, 27, 29-32, 34, and 36-37 were pending and subject to examination. In this Amendment, claims 24 and 26 are canceled, claims 27, 29-32, 34, and 36-37 are amended, and claims 38-41 are added so that claims 27, 29-32, 34, 36-37, and 38-41 are pending and subject to examination on the merits. New claims 38-41 track the language of the previously submitted dependent claims so that no new matter is added.

Claims 27 and 29 are amended so that they are in independent form. The amendments to claims 27 and 29 do not raise new issues requiring further search and/or consideration on the part of the Examiner, and a new ground of rejection would not be appropriate as to amended claims 27 and 29.

35 USC 102 - Shrier et al.

In the Office Action, claims 24, 26, 27, 31, 32, 34, and 37 are rejected as anticipated by Shrier et al. (US 2002/0050912). This rejection is traversed.

Shrier et al. fails to teach or suggest a method including, *inter alia*, "(a) forming a carrier, wherein forming the carrier comprises providing a metal layer, and forming a plurality of bumps in the metal layer ...(b) attaching a semiconductor die to the metal layer after forming the plurality of bumps wherein attaching comprises: attaching the semiconductor die to a die attach region of the carrier, and wherein the plurality of bumps is disposed around the semiconductor die." as recited in independent claim 27. (emphasis added.)

In claim 27, the "carrier" includes a metal layer that has stamped bumps formed in it. A semiconductor die is attached to a die attach region of the carrier. In the Office Action, the Examiner refers to metal layer 103 in FIG. 15 of Shrier et al. as being the "metal layer" in claim 27, and alleges that "Shrier teaches that this type of carrier, and variations thereof, can then be electrically coupled to conductive regions of a circuit substrate of a circuit die, where the bumps will be arranged around the die attach region, as shown in Fig. 6." The metal layer 103 in FIG.

15 of Shrier et al. is part of a device 97 that provides variable voltage protection. The variable voltage protection device is device 25 in Fig. 6 of Shrier et al. Assuming *arguendo* that the variable voltage protection device 25 or a layer therein could even be reasonably called a "carrier" as in independent claim 27, the variable voltage protection device 25 clearly does not have a "die attach region", let alone a semiconductor die that is attached to the die attach region. Shrier et al. also fails to provide any motivation for modifying the disclosed variable voltage protection device to include a "die attach region", let alone a semiconductor die that is attached to the die attach region of a carrier. In Shrier et al., the chip carrier 27 has a die attach region, but the chip carrier 27 is completely separate from the variable voltage protection device 25 with the alleged "bumps". Accordingly, Shrier et al. does not anticipate or obviate independent claim 27 or dependents thereon. Withdrawal of the anticipation rejection is requested.

35 USC 103 - Shrier et al. and Takeda et al.

In the Office Action, claims 24, 26, 27, 29-32, 34, 35, and 36 are rejected as obvious over Shrier et al. and Takeda et al. (U.S. Patent No. 5,892,271).

A. All claim limitations are not taught or suggested by Shrier et al. and Takeda et al.

With respect to independent claim 27, Applicant has already explained why Shrier et al. fails to teach or suggest the invention of independent claim 27. Takeda et al. is allegedly cited for its teaching of copper and conical bumps. Takeda et al. fails to remedy the deficiencies of Shrier et al.

With respect to independent claim 29, neither Shrier et al. nor Takeda et al. teach or suggest a method for forming a carrier for a semiconductor die package, "the method comprising: (a) providing a metal layer; and (b) forming a plurality of bumps in the metal layer, wherein the formed bumps are capable of being electrically coupled to conductive regions of a circuit substrate, and wherein forming the plurality of bumps comprises stamping, wherein the bumps each have a conical shape." (emphasis added.)

Takeda et al. is alleged to teach conical bumps. Takeda et al. describes raised bump portions as "metal projection bumps 3" (c. 3, l. 59). It is unclear how the Examiner can allege that Takeda et al.'s bumps "can be considered to be conical" when the words "conical" or "cone" are nowhere in Takeda et al. One definition of a "cone" is a "solid bounded by a circular or other closed plane base and the surface formed by line segments joining every point of the boundary of the base to a common vertex". *Webster's Ninth Collegiate Dictionary*. Neither Takeda et al.'s drawings nor written description teaches or suggests bumps that are "conical".

The Examiner states that "the raised bump portions of the metal layer (8) shown in Fig. 4 of Takeda et al., can be considered to be conical in shape. That is, they taper from a wider base portion to a narrower top portion approaching an apex, which is a characteristic feature of a conical shape." Even if the Examiner's allegation that each of Takeda et al.'s bumps "taper from a wider base portion to a narrower top portion approaching an apex" is correct, "tapered" bumps are not necessarily "conical". For example, a bent metal ribbon can "taper from a wider base portion to a narrower top portion approaching an apex", but would not be "conical". As noted above, a "cone" refers to a specific shape and is not synonymous with "tapered".

Neither Shrier et al. nor Takeda et al. teach or suggest "conical" bumps, and the Office Action provides no reason or explanation as to why one skilled in the art would have been motivated to modify these references to include "conical bumps". Accordingly, Applicant submits that the obviousness rejection is improper and withdrawal of the rejection is requested.

B. Improper hindsight was used to combine Shrier et al. and Takeda et al.

As noted above, Shrier et al. teaches a "variable voltage protection structure" that is supposed to be attached to a chip carrier (see Fig. 6 of Shrier et al.). Takeda et al. teaches a semiconductor device including a flexible substrate including metal projection bumps. The flexible substrate has a chip 1 mounted to it. Shrier et al.'s variable voltage protection structure is for attachment to a chip carrier, while Takeda et al.'s flexible substrate is itself a chip carrier. One viewing only Shrier et al. and Takeda et al. would not have combined these references in the manner that is proposed by the Examiner, since the cited devices in Shrier et al. and Takeda et al.

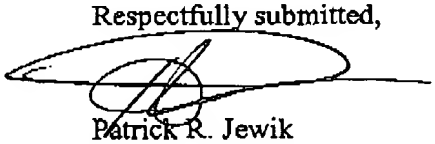
are structurally very different and have distinct and different purposes (*i.e.*, Shier et al.'s invention is used to provide for overvoltage protection whereas Takeda et al.'s invention is used to support a chip). Since one would not have combined these references in the manner proposed by the Examiner by viewing only these references and *without the benefit of Applicant's disclosure*, improper hindsight was used to combine the cited references and the rejection is improper.

CONCLUSION

In view of the foregoing, Applicant believes that there are many more reasons why the claims in this application would be considered allowable, rather than not allowable. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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